

Appendix A
Clean Version of All Currently Pending Claims

- Sub E1*
1. A single-chip integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:
 - memory, including one or more memory arrays for storing information related to the transceiver;
 - analog to digital conversion circuitry for receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;
 - control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory;
 - an interface for allowing a host to read directly from and write directly to locations within the memory; and
 - comparison logic for comparing the digital values with limit values to generate flag values, wherein the flag values are stored in predefined locations within the memory during operation of the optoelectronic transceiver.
 2. The single-chip integrated circuit of claim 1, further including:
 - a cumulative clock for generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable via the interface.
 3. The single-chip integrated circuit of claim 1, further including:
 - a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.
 4. The single-chip integrated circuit of claim 1, further including:
 - a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

5. The single-chip integrated circuit of claim 4, further including:
a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.
6. The single-chip integrated circuit of claim 5, wherein
the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and
the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.
7. The single-chip integrated circuit of claim 4, wherein
the comparison logic includes logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.
8. The single-chip integrated circuit of claim 1, further including:
a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.
9. The single-chip integrated circuit of claim 8, wherein
the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the

digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

10. The single-chip integrated circuit of claim 1, further including fault handling logic, coupled to the transceiver for receiving at least one fault signal from the transceiver, coupled to the memory to receive at least one flag value stored in the memory, and coupled to a host interface to transmit a computed fault signal, the fault handling logic including computational logic for logically combining the at least one fault signal received from the transceiver and the at least one flag value received from the memory to generate the computed fault signal.

11. The single-chip integrated circuit of claim 1, further including control adjustment circuitry for adjusting a first control signal of the control signals generated by the control circuitry in accordance with an adjustment value stored in the memory.

12. The single-chip integrated circuit of claim 1, wherein the control circuitry generates the first control signal in accordance with a temperature.

13. The single-chip integrated circuit of claim 1, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

14. A single-chip integrated circuit for monitoring an optoelectronic device, comprising:
memory, including one or more memory arrays for storing information related to the optoelectronic device;

analog to digital conversion circuitry for receiving a plurality of analog signals from the optoelectronic device, the analog signals corresponding to operating conditions of the optoelectronic device, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory; and

a memory interface for allowing a host to read directly from and write directly to locations within the memory in accordance with commands received from a host device.

15. The single-chip integrated circuit of claim 14, further including:

a cumulative clock for generating a time value corresponding to cumulative operation time of the optoelectronic device, wherein the generated time value is readable via the memory interface.

16. The single-chip integrated circuit of claim 14, further including:

a cumulative clock for generating and storing in a register a time value corresponding to cumulative operation time of the optoelectronic device, wherein the register in which the time value is stored comprises one of the memory arrays of the memory.

17. The single-chip integrated circuit of claim 14, further including:

a power supply voltage sensor coupled to the analog to digital conversion circuitry, the power supply voltage sensor generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the power level signal into a digital power level value and to store the digital power level value in a predefined power level location within the memory.

18. The single-chip integrated circuit of claim 17, further including:

comparison logic for comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

17. 18. The single-chip integrated circuit of claim 18, further including

a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.

18. 19. The single-chip integrated circuit of claim 19, wherein

the comparison logic includes logic for comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

- Sub E1*
- ~~21. The single-chip integrated circuit of claim 14, further including
a temperature sensor coupled to the analog to digital conversion circuitry, the
temperature sensor generating a temperature signal corresponding to a temperature of the
optoelectronic device, wherein the analog to digital conversion circuitry is configured to
convert the temperature signal into a digital temperature value and to store the digital
temperature value in a predefined temperature location within the memory.~~
- ~~22. The single-chip integrated circuit of claim 21, further including
comparison logic for comparing the digital temperature value with a temperature limit
value, generating a temperature flag value based on the comparison of the digital temperature
signal with the temperature limit value, and storing the temperature flag value in a predefined
temperature flag location within the memory.~~
- Sub E1*
- ~~23. The single-chip integrated circuit of claim 14, further including
fault handling logic, coupled to the optoelectronic device for receiving at least one
fault signal from the optoelectronic device, coupled to the memory to receive at least one flag
value stored in the memory, and coupled to a host interface to transmit a computed fault
signal, the fault handling logic including computational logic for logically combining the at
least one fault signal received from the optoelectronic device and the at least one flag value
received from the memory to generate the computed fault signal.~~
- Sub E1*
- ~~24. The single-chip integrated circuit of claim 14, wherein the plurality of analog signals
includes two analog signals selected from the set consisting of laser bias current, laser output
power, and received power.~~
- Sub E1*
- ~~25. A single-chip integrated circuit for controlling an optoelectronic transceiver having a
laser transmitter and a photodiode receiver, comprising:
analog to digital conversion circuitry for receiving a plurality of analog signals from
the laser transmitter and photodiode receiver, converting the received analog signals into
digital values, and storing the digital values in predefined memory mapped locations within
the integrated circuit;
comparison logic for comparing the digital values with limit values to generate flag
values, wherein the flag values are stored in predefined memory mapped locations within the
integrated circuit during operation of the optoelectronic transceiver;~~

control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the integrated circuit; and
a memory mapped interface for allowing a host to read directly from and write directly to locations within the integrated circuit and for accessing memory mapped locations within the integrated circuit for controlling operation of the control circuitry.

22.

26. A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a memory; and

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined locations within the memory;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined locations within the memory during operation of the optoelectronic transceiver;

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory.

23.

27. The method of claim *26*, further including:

generating a time value corresponding to cumulative operation time of the transceiver, wherein the generated time value is readable by the host device via a memory interface.

24.

28. The method of claim *26*, further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a location in the memory.

25.

29. The method of claim *26*, further including:

converting an analog power supply voltage level signal, corresponding to a voltage level of the transceiver, into a digital power level value and storing the digital power level value in a predefined power level location within the memory.

26.

30. The method of claim *29*, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

27.

26

31. The method of claim 30, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory; and

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

28.

32. The method integrated circuit of claim 29, including

comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.

29.

33. The method of claim 26, further including:

generating a temperature signal corresponding to a temperature of the transceiver, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.

30.

34. The method of claim 33, including:

comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.

31.

35. The method of 26, further including

receiving at least one fault signal from the transceiver, receiving at least one flag value stored in the memory, logically combining the at least one fault signal received from

the transceiver and the at least one flag value received from the memory to generate a computed fault signal, and transmitting the computed fault signal to the host device.

- ~~32.~~ ²² ~~36.~~ The method of claim ~~26~~, further including
adjusting a first control signal of the control signals in accordance with an adjustment value stored in the memory.
- ~~33.~~ ²² ~~37.~~ The method of claim ~~26~~, wherein the method is performed by a single-chip controller integrated circuit.
- ~~34.~~ ²² ~~38.~~ The method of claim ~~26~~, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

Sub 1
Sub 2
X
Sub 3
Sub 4
Sub 5
Sub 6
Sub 7
Sub 8
Sub 9
Sub 10
Sub 11
Sub 12
Sub 13
Sub 14
Sub 15
Sub 16
Sub 17
Sub 18
Sub 19
Sub 20
Sub 21
Sub 22
Sub 23
Sub 24
Sub 25
Sub 26
Sub 27
Sub 28
Sub 29
Sub 30
Sub 31
Sub 32
Sub 33
Sub 34
Sub 35
Sub 36
Sub 37
Sub 38
Sub 39
Sub 40
Sub 41
Sub 42
Sub 43
Sub 44
Sub 45
Sub 46
Sub 47
Sub 48
Sub 49
Sub 50
Sub 51
Sub 52
Sub 53
Sub 54
Sub 55
Sub 56
Sub 57
Sub 58
Sub 59
Sub 60
Sub 61
Sub 62
Sub 63
Sub 64
Sub 65
Sub 66
Sub 67
Sub 68
Sub 69
Sub 70
Sub 71
Sub 72
Sub 73
Sub 74
Sub 75
Sub 76
Sub 77
Sub 78
Sub 79
Sub 80
Sub 81
Sub 82
Sub 83
Sub 84
Sub 85
Sub 86
Sub 87
Sub 88
Sub 89
Sub 90
Sub 91
Sub 92
Sub 93
Sub 94
Sub 95
Sub 96
Sub 97
Sub 98
Sub 99
Sub 100
Sub 101
Sub 102
Sub 103
Sub 104
Sub 105
Sub 106
Sub 107
Sub 108
Sub 109
Sub 110
Sub 111
Sub 112
Sub 113
Sub 114
Sub 115
Sub 116
Sub 117
Sub 118
Sub 119
Sub 120
Sub 121
Sub 122
Sub 123
Sub 124
Sub 125
Sub 126
Sub 127
Sub 128
Sub 129
Sub 130
Sub 131
Sub 132
Sub 133
Sub 134
Sub 135
Sub 136
Sub 137
Sub 138
Sub 139
Sub 140
Sub 141
Sub 142
Sub 143
Sub 144
Sub 145
Sub 146
Sub 147
Sub 148
Sub 149
Sub 150
Sub 151
Sub 152
Sub 153
Sub 154
Sub 155
Sub 156
Sub 157
Sub 158
Sub 159
Sub 160
Sub 161
Sub 162
Sub 163
Sub 164
Sub 165
Sub 166
Sub 167
Sub 168
Sub 169
Sub 170
Sub 171
Sub 172
Sub 173
Sub 174
Sub 175
Sub 176
Sub 177
Sub 178
Sub 179
Sub 180
Sub 181
Sub 182
Sub 183
Sub 184
Sub 185
Sub 186
Sub 187
Sub 188
Sub 189
Sub 190
Sub 191
Sub 192
Sub 193
Sub 194
Sub 195
Sub 196
Sub 197
Sub 198
Sub 199
Sub 200
Sub 201
Sub 202
Sub 203
Sub 204
Sub 205
Sub 206
Sub 207
Sub 208
Sub 209
Sub 210
Sub 211
Sub 212
Sub 213
Sub 214
Sub 215
Sub 216
Sub 217
Sub 218
Sub 219
Sub 220
Sub 221
Sub 222
Sub 223
Sub 224
Sub 225
Sub 226
Sub 227
Sub 228
Sub 229
Sub 230
Sub 231
Sub 232
Sub 233
Sub 234
Sub 235
Sub 236
Sub 237
Sub 238
Sub 239
Sub 240
Sub 241
Sub 242
Sub 243
Sub 244
Sub 245
Sub 246
Sub 247
Sub 248
Sub 249
Sub 250
Sub 251
Sub 252
Sub 253
Sub 254
Sub 255
Sub 256
Sub 257
Sub 258
Sub 259
Sub 260
Sub 261
Sub 262
Sub 263
Sub 264
Sub 265
Sub 266
Sub 267
Sub 268
Sub 269
Sub 270
Sub 271
Sub 272
Sub 273
Sub 274
Sub 275
Sub 276
Sub 277
Sub 278
Sub 279
Sub 280
Sub 281
Sub 282
Sub 283
Sub 284
Sub 285
Sub 286
Sub 287
Sub 288
Sub 289
Sub 290
Sub 291
Sub 292
Sub 293
Sub 294
Sub 295
Sub 296
Sub 297
Sub 298
Sub 299
Sub 300
Sub 301
Sub 302
Sub 303
Sub 304
Sub 305
Sub 306
Sub 307
Sub 308
Sub 309
Sub 310
Sub 311
Sub 312
Sub 313
Sub 314
Sub 315
Sub 316
Sub 317
Sub 318
Sub 319
Sub 320
Sub 321
Sub 322
Sub 323
Sub 324
Sub 325
Sub 326
Sub 327
Sub 328
Sub 329
Sub 330
Sub 331
Sub 332
Sub 333
Sub 334
Sub 335
Sub 336
Sub 337
Sub 338
Sub 339
Sub 340
Sub 341
Sub 342
Sub 343
Sub 344
Sub 345
Sub 346
Sub 347
Sub 348
Sub 349
Sub 350
Sub 351
Sub 352
Sub 353
Sub 354
Sub 355
Sub 356
Sub 357
Sub 358
Sub 359
Sub 360
Sub 361
Sub 362
Sub 363
Sub 364
Sub 365
Sub 366
Sub 367
Sub 368
Sub 369
Sub 370
Sub 371
Sub 372
Sub 373
Sub 374
Sub 375
Sub 376
Sub 377
Sub 378
Sub 379
Sub 380
Sub 381
Sub 382
Sub 383
Sub 384
Sub 385
Sub 386
Sub 387
Sub 388
Sub 389
Sub 390
Sub 391
Sub 392
Sub 393
Sub 394
Sub 395
Sub 396
Sub 397
Sub 398
Sub 399
Sub 400
Sub 401
Sub 402
Sub 403
Sub 404
Sub 405
Sub 406
Sub 407
Sub 408
Sub 409
Sub 410
Sub 411
Sub 412
Sub 413
Sub 414
Sub 415
Sub 416
Sub 417
Sub 418
Sub 419
Sub 420
Sub 421
Sub 422
Sub 423
Sub 424
Sub 425
Sub 426
Sub 427
Sub 428
Sub 429
Sub 430
Sub 431
Sub 432
Sub 433
Sub 434
Sub 435
Sub 436
Sub 437
Sub 438
Sub 439
Sub 440
Sub 441
Sub 442
Sub 443
Sub 444
Sub 445
Sub 446
Sub 447
Sub 448
Sub 449
Sub 450
Sub 451
Sub 452
Sub 453
Sub 454
Sub 455
Sub 456
Sub 457
Sub 458
Sub 459
Sub 460
Sub 461
Sub 462
Sub 463
Sub 464
Sub 465
Sub 466
Sub 467
Sub 468
Sub 469
Sub 470
Sub 471
Sub 472
Sub 473
Sub 474
Sub 475
Sub 476
Sub 477
Sub 478
Sub 479
Sub 480
Sub 481
Sub 482
Sub 483
Sub 484
Sub 485
Sub 486
Sub 487
Sub 488
Sub 489
Sub 490
Sub 491
Sub 492
Sub 493
Sub 494
Sub 495
Sub 496
Sub 497
Sub 498
Sub 499
Sub 500
Sub 501
Sub 502
Sub 503
Sub 504
Sub 505
Sub 506
Sub 507
Sub 508
Sub 509
Sub 510
Sub 511
Sub 512
Sub 513
Sub 514
Sub 515
Sub 516
Sub 517
Sub 518
Sub 519
Sub 520
Sub 521
Sub 522
Sub 523
Sub 524
Sub 525
Sub 526
Sub 527
Sub 528
Sub 529
Sub 530
Sub 531
Sub 532
Sub 533
Sub 534
Sub 535
Sub 536
Sub 537
Sub 538
Sub 539
Sub 540
Sub 541
Sub 542
Sub 543
Sub 544
Sub 545
Sub 546
Sub 547
Sub 548
Sub 549
Sub 550
Sub 551
Sub 552
Sub 553
Sub 554
Sub 555
Sub 556
Sub 557
Sub 558
Sub 559
Sub 560
Sub 561
Sub 562
Sub 563
Sub 564
Sub 565
Sub 566
Sub 567
Sub 568
Sub 569
Sub 570
Sub 571
Sub 572
Sub 573
Sub 574
Sub 575
Sub 576
Sub 577
Sub 578
Sub 579
Sub 580
Sub 581
Sub 582
Sub 583
Sub 584
Sub 585
Sub 586
Sub 587
Sub 588
Sub 589
Sub 590
Sub 591
Sub 592
Sub 593
Sub 594
Sub 595
Sub 596
Sub 597
Sub 598
Sub 599
Sub 600
Sub 601
Sub 602
Sub 603
Sub 604
Sub 605
Sub 606
Sub 607
Sub 608
Sub 609
Sub 610
Sub 611
Sub 612
Sub 613
Sub 614
Sub 615
Sub 616
Sub 617
Sub 618
Sub 619
Sub 620
Sub 621
Sub 622
Sub 623
Sub 624
Sub 625
Sub 626
Sub 627
Sub 628
Sub 629
Sub 630
Sub 631
Sub 632
Sub 633
Sub 634
Sub 635
Sub 636
Sub 637
Sub 638
Sub 639
Sub 640
Sub 641
Sub 642
Sub 643
Sub 644
Sub 645
Sub 646
Sub 647
Sub 648
Sub 649
Sub 650
Sub 651
Sub 652
Sub 653
Sub 654
Sub 655
Sub 656
Sub 657
Sub 658
Sub 659
Sub 660
Sub 661
Sub 662
Sub 663
Sub 664
Sub 665
Sub 666
Sub 667
Sub 668
Sub 669
Sub 670
Sub 671
Sub 672
Sub 673
Sub 674
Sub 675
Sub 676
Sub 677
Sub 678
Sub 679
Sub 680
Sub 681
Sub 682
Sub 683
Sub 684
Sub 685
Sub 686
Sub 687
Sub 688
Sub 689
Sub 690
Sub 691
Sub 692
Sub 693
Sub 694
Sub 695
Sub 696
Sub 697
Sub 698
Sub 699
Sub 700
Sub 701
Sub 702
Sub 703
Sub 704
Sub 705
Sub 706
Sub 707
Sub 708
Sub 709
Sub 710
Sub 711
Sub 712
Sub 713
Sub 714
Sub 715
Sub 716
Sub 717
Sub 718
Sub 719
Sub 720
Sub 721
Sub 722
Sub 723
Sub 724
Sub 725
Sub 726
Sub 727
Sub 728
Sub 729
Sub 730
Sub 731
Sub 732
Sub 733
Sub 734
Sub 735
Sub 736
Sub 737
Sub 738
Sub 739
Sub 740
Sub 741
Sub 742
Sub 743
Sub 744
Sub 745
Sub 746
Sub 747
Sub 748
Sub 749
Sub 750
Sub 751
Sub 752
Sub 753
Sub 754
Sub 755
Sub 756
Sub 757
Sub 758
Sub 759
Sub 760
Sub 761
Sub 762
Sub 763
Sub 764
Sub 765
Sub 766
Sub 767
Sub 768
Sub 769
Sub 770
Sub 771
Sub 772
Sub 773
Sub 774
Sub 775
Sub 776
Sub 777
Sub 778
Sub 779
Sub 780
Sub 781
Sub 782
Sub 783
Sub 784
Sub 785
Sub 786
Sub 787
Sub 788
Sub 789
Sub 790
Sub 791
Sub 792
Sub 793
Sub 794
Sub 795
Sub 796
Sub 797
Sub 798
Sub 799
Sub 800
Sub 801
Sub 802
Sub 803
Sub 804
Sub 805
Sub 806
Sub 807
Sub 808
Sub 809
Sub 810
Sub 811
Sub 812
Sub 813
Sub 814
Sub 815
Sub 816
Sub 817
Sub 818
Sub 819
Sub 820
Sub 821
Sub 822
Sub 823
Sub 824
Sub 825
Sub 826
Sub 827
Sub 828
Sub 829
Sub 830
Sub 831
Sub 832
Sub 833
Sub 834
Sub 835
Sub 836
Sub 837
Sub 838
Sub 839
Sub 840
Sub 841
Sub 842
Sub 843
Sub 844
Sub 845
Sub 846
Sub 847
Sub 848
Sub 849
Sub 850
Sub 851
Sub 852
Sub 853
Sub 854
Sub 855
Sub 856
Sub 857
Sub 858
Sub 859
Sub 860
Sub 861
Sub 862
Sub 863
Sub 864
Sub 865
Sub 866
Sub 867
Sub 868
Sub 869
Sub 870
Sub 871
Sub 872
Sub 873
Sub 874
Sub 875
Sub 876
Sub 877
Sub 878
Sub 879
Sub 880
Sub 881
Sub 882
Sub 883
Sub 884
Sub 885
Sub 886
Sub 887
Sub 888
Sub 889
Sub 890
Sub 891
Sub 892
Sub 893
Sub 894
Sub 895
Sub 896
Sub 897
Sub 898
Sub 899
Sub 900
Sub 901
Sub 902
Sub 903
Sub 904
Sub 905
Sub 906
Sub 907
Sub 908
Sub 909
Sub 910
Sub 911
Sub 912
Sub 913
Sub 914
Sub 915
Sub 916
Sub 917
Sub 918
Sub 919
Sub 920
Sub 921
Sub 922
Sub 923
Sub 924
Sub 925
Sub 926
Sub 927
Sub 928
Sub 929
Sub 930
Sub 931
Sub 932
Sub

~~generating a power level signal corresponding to a power supply voltage level of the optoelectronic device, converting the power level signal into a digital power level value and storing the digital power level value in a predefined power level location within the memory.~~

~~43. The method of claim 39, further including:~~

~~comparing the digital power level value with a power level limit value, generating a power level flag value based on the comparison of the digital power level signal with the power level limit value, and storing the power level flag value in a predefined power level flag location within the memory.~~

~~38.~~

~~35
39~~

~~44. The method of claim 43, further including~~

~~generating a temperature signal corresponding to a temperature of the optoelectronic device, converting the temperature signal into a digital temperature value and storing the digital temperature value in a predefined temperature location within the memory.~~

~~39.~~

~~38~~

~~45. The method of claim 44, wherein~~

~~comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.~~

~~46. The method of claim 39, further including~~

~~generating a temperature signal corresponding to a temperature of the optoelectronic device, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in a predefined temperature location within the memory.~~

~~47. The method of claim 46, further including~~

~~comparing the digital temperature value with a temperature limit value, generating a temperature flag value based on the comparison of the digital temperature signal with the temperature limit value, and storing the temperature flag value in a predefined temperature flag location within the memory.~~

~~40.~~

~~35~~

~~48. The method of claim 39, further including~~

receiving at least one fault signal from the optoelectronic device, receiving at least one flag value stored in the memory, logically combining the at least one fault signal received from the optoelectronic device and the at least one flag value received from the memory to generate a computed fault signal, and transmit the computed fault signal to the host device.

~~41.~~ ~~49.~~ The method of claim ~~39~~ ³⁵, wherein the plurality of analog signals includes two analog signals selected from the set consisting of laser bias current, laser output power, and received power.

~~42.~~ ~~50.~~ A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:

in accordance with instructions received from a host device, enabling the host device to read directly from and write directly to locations within a controller of the optoelectronic transceiver;

receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in predefined memory mapped locations within the controller;

comparing the digital values with limit values to generate flag values, and storing the flag values in predefined memory mapped locations within the controller during operation of the optoelectronic transceiver; and

generating control signals to control operation of the laser transmitter in accordance with one or more values stored in the predefined memory mapped locations within the controller.

~~43.~~ ~~51.~~ The method of claim ~~50~~ ⁴², further including:

generating and storing in a register a time value corresponding to cumulative operation time of the transceiver, wherein the register in which the time value is accessed by the reading step as a memory mapped within the controller.

~~52.~~ ~~A single-chip integrated circuit for monitoring an optoelectronic device, comprising:~~
~~memory, including one or more memory arrays for storing information related to the optoelectronic device;~~

~~analog to digital conversion circuitry configured to receive a plurality of analog signals, the analog signals corresponding to operating conditions of the optoelectronic device,~~

~~converting at least one of the received analog signals into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and~~

~~a memory interface for allowing a host device to read directly from and write directly to locations within the memory in accordance with commands received from a host device.~~

53. The single-chip integrated circuit of claim 52, further including:

~~a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory.~~

54. The single-chip integrated circuit of claim 52, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the single-chip integrated circuit, wherein the analog to digital conversion circuitry is configured to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory.

55. A single-chip integrated circuit for monitoring an optoelectronic device, comprising:
~~memory, including one or more memory arrays for storing information related to the optoelectronic device;~~

~~analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic device, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and~~

~~a memory interface for allowing a host device to read directly from and write directly to locations within the memory in accordance with commands received from a host device.~~

56. The single-chip integrated circuit of claim 55, further including:

~~a temperature sensor coupled to the analog to digital conversion circuitry, the temperature sensor generating a temperature signal corresponding to a temperature of the transceiver, wherein the analog to digital conversion circuitry is configured to convert the~~

~~temperature signal into a digital temperature value and to store the digital temperature value in the at least one predefined location within the memory.~~

57. The single-chip integrated circuit of claim 55, further including control circuitry, responsive to the digital temperature digital value for controlling operation of the optoelectronic device.

58. The single-chip integrated circuit of claim 55, wherein the analog to digital conversion circuitry is configured to receive a voltage signal from a source external to the single-chip integrated circuit, wherein the analog to digital conversion circuitry is configured to convert the voltage signal into a digital voltage value and to store the digital voltage value in the at least one predefined location within the memory.

59. The single-chip integrated circuit of claim 55, further including control circuitry, responsive to the at least one digital value for controlling operation of the optoelectronic device.

60. A method of monitoring an optoelectronic device, comprising:
storing, in one or more memory arrays, information related to the optoelectronic device;
receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic device;
converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one predefined location within the memory; and
reading directly from and writing directly to locations within the memory in accordance with commands received from a host device.

61. The method of claim 60, further including:
generating a temperature signal corresponding to a temperature of the transceiver;
the converting and storing steps including converting the temperature signal into a digital temperature value, and storing the digital temperature value in the at least one predefined location within the memory.

62. The method of claim 61, further including controlling operation of the optoelectronic device in response to the digital temperature value.

63. ~~The method of claim 60, wherein~~

~~the receiving step includes receiving a voltage signal from a source external to the single-chip integrated circuit,~~

~~the converting and storing steps include converting the voltage signal into a digital voltage value and storing the digital voltage value in the at least one predefined location within the memory.~~

64. ~~The method of claim 60, further including controlling operation of the optoelectronic device in response to the at least one digital value.~~